January-2005

BREL International

Application Notes-MLCC Capacitors

CHIP SELECTION

Multilayer capacitors (MLCC) are categorized by dielectric performance with temperature, or “temperature coefficient”, as these devices vary in behavior over temperature. The choice of component is thus largely determined by the temperature stability required of the device, i.e. type of dielectric, and the size necessary for a given capacitance and voltage rating. The following items are pertinent to chip selection:

DIELECTRIC TYPE

COG: Ultra stable Class I dielectric, with negligible dependence of electrical properties on temperature, voltage, frequency and time. This dielectric is used in circuitry requiring very stable performance.
X7R: Stable Class II dielectric, with predictable change in properties with temperature, voltage, frequency and time. Used as blocking, de-coupling, bypassing and frequency discriminating elements. This dielectric is ferroelectric, and provides higher capacitance than Class I.
Z5U/Y5V: General purpose Class III dielectrics with higher dielectric constant and greater variation of properties with temperature and test conditions. Very high capacitance per unit volume is attainable for general purpose applications where stability is not important.

CAPACITOR SIZE

Size selection is based primarily on capacitance value and voltage rating. Smaller units are generally less expensive; 0805 is the most economical size. Because mass affects the thermal shock behavior of chips, size selection must consider the soldering method used to attach the chip to the board. Sizes 1812 and smaller can be wave, vapor phase or reflow soldered. Larger units require reflow soldering.

TERMINATION MATERIAL

Nickel barrier termination, with exceptional solder leach resistance is recommended for all applications involving solder. BREL International offers two versions of the nickel barrier termination. The "N" termination is a nickel barrier with 100% matte tin for a lead free capacitor. The "Y" termination is a nickel barrier with 90/10 tin/lead for military applications. Silver palladium termination is required for epoxy attachment, also for solder reflow below 230°C. Silver termination, which is most ductile, yet leaches readily in solder, is often preferred for units to be leaded, to minimize thermal cycle stresses.

PACKAGING

Units are available in bulk, reeled or in waffle pack. Bar coding is standard for bulk and reeled packaging.

ATTACHMENT METHODS

Bonding of capacitors to substrates can be categorized into two methods, those involving solder, which are prevalent, and those using other materials, such as epoxies and thermo-compression or ultrasonic bonding with wire.

SOLDERING

Soldering methods commonly used in the industry and recommended are Reflow Soldering, Wave Soldering, and to a lesser extent, Vapor Phase Soldering. All these methods involve thermal cycling of the components and therefore the rate of heating and cooling must be controlled to preclude thermal shocking of the devices. In general, rates which do not exceed 120°C per minute and a ΔT spike of 100°C maximum for any soldering process on sizes 1812 and smaller is advisable. Other precautions include post soldering handling, primarily avoidance of rapid cooling with contact with heat sinks, such as conveyors or cleaning solutions. Large chips are more prone to thermal shock as their greater bulk will result in sharper thermal gradients within the device during thermal cycling. Units larger than 1812 experience excessive stress if processed through the fast cycles typical of solder wave or vapor phase operations. Solder reflow is most applicable to the larger chips as the rates of heating and cooling can be slowed within safe limits. In general, rates that do not exceed 60°C per minute and a ΔT spike of 50°C maximum for any soldering process on sizes larger than 1812 is advisable. Attachment using a soldering iron requires extra care, particularly with large components, as thermal gradients are not easily controlled and may cause cracking of the chip. Precautions include preheating of the assembly to within 100°C of the solder flow temperature, the use of a fine tip iron which does not exceed 30 watts and limitation of contact of the iron to the circuit pad areas only.

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Issue: January-2005

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BONDING

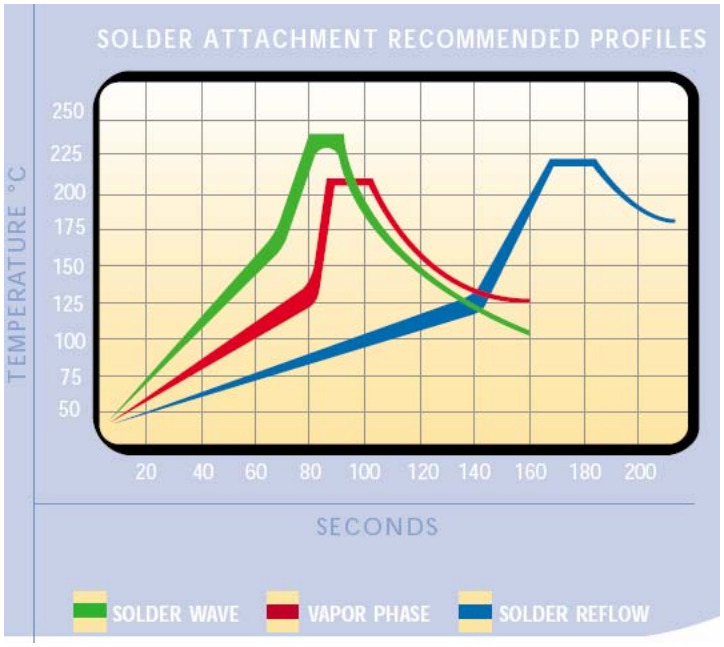
Hybrid assembly using conductive epoxy or wire bonding requires the use of silver palladium or gold terminations. Nickel barrier termination is not practical in these applications, as intermetallics will form between the dissimilar metals. The ESR will increase over time and may eventually break contact when exposed to temperature cycling

CLEANING

Chip capacitors can withstand common agents such as water, alcohol and degreaser solvents used for cleaning boards. Ascertain that no flux residues are left on the chip surfaces as these diminish electrical performance.

BOARD DESIGN CONSIDERATIONS

The amount of solder applied to the chip capacitor will influence the reliability of the device. Excessive solder can create thermal and tensile stresses on the component which could lead to fracturing of the chip or the solder joint itself. Insufficient or uneven solder application can result in weak bonds, rotation of the device off line or lifting of one terminal off the pad (tombstoning). The volume of solder is process and board pad size dependent. WAVE SOLDERING exposes the devices to a large solder volume; hence the pad size area must be restricted to accept an amount of solder which is not detrimental to the chip size utilized. Typically the pad width is 66% of the component width, and the length is .030" (.760 mm) longer than the termination band on the chip. A 0805 chip which is .050" wide and has a .020" termination band therefore requires a pad .033" wide by .050" in length. Opposing pads should be identical in size to preclude uneven solder fillets and mismatched surface tension forces which can misalign the device. It is preferred that the pad layout results in alignment of the long axis of the chips at right angles to the solder wave, to promote even wetting of all terminals. Orientation of components in line with the board travel direction may require dual waves with solder turbulence to preclude cold solder joints on the trailing terminals of the devices, as these are blocked from full exposure to the solder by the body of the capacitor. Restrictions in chip alignment do not apply to SOLDER REFLOW or VAPOR PHASE processes, where the solder volume is controlled by the solder paste deposition on the circuit pads. BREL International has adopted the IPC-SM-782 methodology for solder reflow land patterns. The BREL International recommended solder pads brochure is available for reference on the BREL International Website.



RECOMMENDATIONS

Preheat/Cooling rates not to exceed 120°C/minute with □T spikes to max temperature not to exceed 100ºC for 1812 size and smaller. Preheat/Cooling rates not to exceed 60°C /minute for over 1812 size.

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